SPECIFICATION
FOR
LCM Module

MODULE No:	KD020LQRMA017
CUSTOMER:	

STARTEK	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

Revision History

Date	Rev. No.	Page	Summary
2020.04.02	V1.0	ALL	FIRST ISSUE

Contents

* Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorpho us silicon TFT as a switching device. This module is composed of a transflective type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 2.0 " TFT-LCD contains 320x240 pixels, and can dis play up to 65K/262K colors.

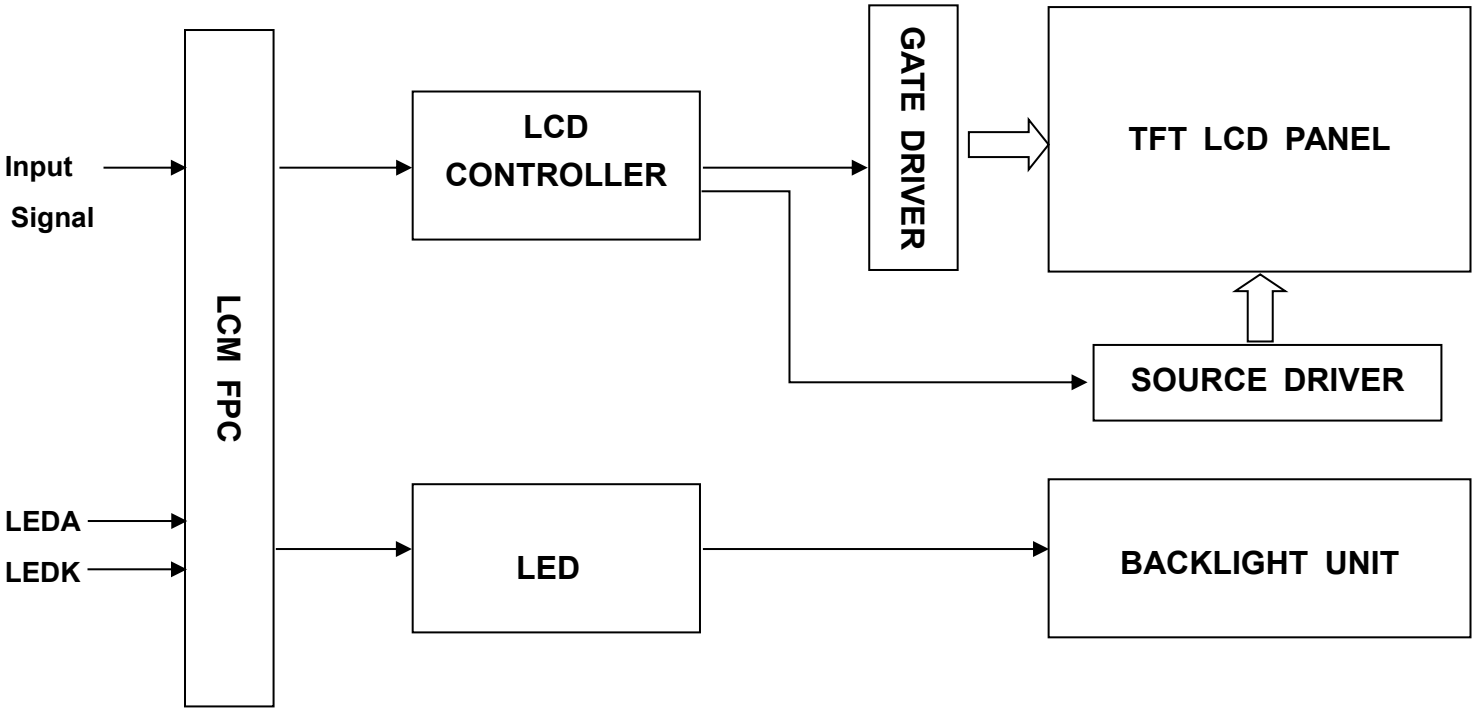
* Features

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	40.80(H)*30.60(V) (2.0 inch)	mm	
Driver element	TFT active matrix	-	
Display colors	65K/262K	colors	
Number of pixels	320(RGB)*240	dots	
Pixel arrangement	RGB vertical stripe	-	
Pixel pitch	0.1275(H)*0.1275(V)	mm	
Viewing angle	Wide angle	o'clock	
Controller IC	ILI9342C	-	
LCM Interface	8/9/16/18Bit MCU 3/4SPI+16/18Bit RGB Interface 3-line/4-line Serial	-	
Display mode	Transflective /Normally Black	-	
Operating temperature	-20～+70	℃	
Storage temperature	-30～+80	℃	

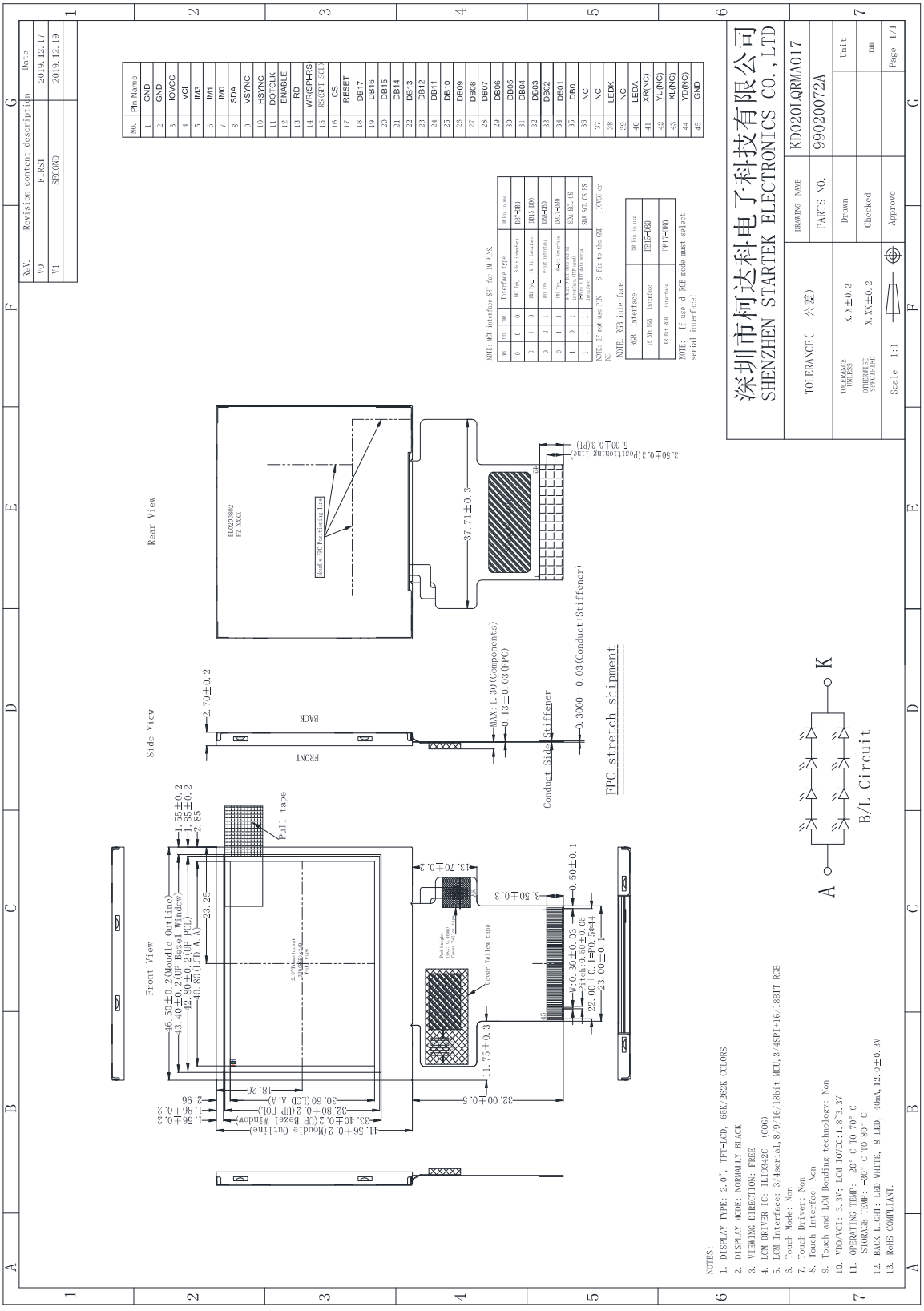
* Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)	-	46.50	-	mm	
	Vertical(V)	-	41.56	-	mm	
	Depth(D)	-	2.7	-	mm	
Weight		-	10	-	g	

1. Block Diagram



2. Outline dimension



3. Input terminal Pin Assignment

<table>
<tr><th>NO.</th><th>SYMBOL</th><th>DISCRIPTION</th><th>I/O</th></tr>
<tr><td>1</td><td>GND</td><td>Ground.</td><td>P</td></tr>
<tr><td>2</td><td>GND</td><td>Ground.</td><td>P</td></tr>
<tr><td>3</td><td>IOVCC</td><td>Supply voltage(1.65-3.3V)</td><td>P</td></tr>
<tr><td>4</td><td>VCI</td><td>Supply voltage(3.3V).</td><td>P</td></tr>
<tr><td>5</td><td>IM3</td><td rowspan="3">Interface Selection
<table>
<tr><th>IM3</th><th>IM2</th><th>IM0</th><th>Interface type</th><th>DB Pin in use</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>DBI Tyb_ 8-bit interface</td><td>DB7-DB0</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>DBI Tyb_ 16-bit interface</td><td>DB15-DB0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>DBI Tyb_ 9-bit interface</td><td>DB8-DB0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>DBI Tyb_ 18-bit interface</td><td>DB17-DB0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>3-Wire 9 BIT data serial interface.</td><td>SDA SCL CS</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>4-Wire 8 BIT data serial interface</td><td>SDA SCL CS RS</td></tr>
</table></td><td>I</td></tr>
<tr><td>6</td><td>IM2</td><td>I</td></tr>
<tr><td>7</td><td>IM0</td><td>I</td></tr>
<tr><td>8</td><td>SDA</td><td>Serial input signal.The data is applied on the rising edge of the SCL signal.
If not used, fix this pin at IOVCC or GND.</td><td>I</td></tr>
<tr><td>9</td><td>VSYNC</td><td>Frame synchronizing signal for RGB interface operation.
fix this pin at IOVCC or GND when not in use.</td><td>I</td></tr>
<tr><td>10</td><td>HSYNC</td><td>Line synchronizing signal for RGB interface operation.
fix this pin at IOVCC or GND when not in use</td><td>I</td></tr>
<tr><td>11</td><td>DOTCLK</td><td>Dot clock signal for RGB interface operation
Fix this pin at IOVCC or GND when not in use.</td><td>I</td></tr>
<tr><td>12</td><td>ENABLE</td><td>Data enable signal for RGB interface operation.
fix this pin at IOVCC or GND when not in use.</td><td>I</td></tr>
<tr><td>13</td><td>RD</td><td>Serves as a read signal and MCU read data at the rising edge.
fix this pin at IOVCC or GND when not in use.</td><td>I</td></tr>
<tr><td>14</td><td>WR(SPI-RS)</td><td>(WR): Serves as a write signal and writes data at the rising edge.
4-line system (RS): Serves as command or parameter select.
Fix to IOVCC or GND level when not in use.</td><td>I</td></tr>
<tr><td>15</td><td>RS(SPI-SCL)</td><td>This pin is used to select “Data or Command” in the parallel interface.
When RS = ’1’, data is selected.</td><td>I</td></tr>
</table>

		When RS = '0', command is selected. This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface. If not used, this pin should be connected to IOVCC or GND. RS_SCL1 is equal to RS(SCL).	
16	CS	Chip select input pin ("Low" enable). This pin can be permanently fixed "Low" in MPU interface mode only. CSX1 is equal to CSX.	I
17	RESET	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low. RESX1 is equal to RESX.	I
18-35	DB17-DB0	18-bit parallel bi-directional data bus for MCU system and RGB interface mode Fix to GND level when not in use	I/O
36	NC	--	--
37	NC	--	--
38	LEDK	Cathode pin OF backlight	P
39	NC	--	--
40	LEDA	Anode pin of backlight	P
41	XR	No connected.	
42	YU	No connected.	
43	XL	No connected.	
44	YD	No connected.	
45	GND	Ground.	P

4. LCD Optical Characteristics

4.1 Optical specification

Item		Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio		CR	Θ=0 Normal viewing angle	120	170	--		(1)(2)
Reflection Ratio （With Polarizer）		R		5	7	--	%	
Reflective Contrast Ratio		Cr		--	5	--	%	
Response time	Rising	$T_{R+}T_F$		--	30	50	msec	(1)(3)
	Falling							
Color Gamut		S(%)		37	42	--	%	
Color Filter Chromacicity	White	W_X		0.2517	0.2917	0.3317		(1)(4) CA-310
		W_Y		0.2626	0.3026	0.3426		
	Red	R_X		0.5101	0.5501	0.5901		
		R_Y		0.3079	0.3479	0.3879		
	Green	G_X		0.2931	0.3331	0.3731		
		G_Y		0.4998	0.5398	0.5798		
	Blue	B_X		0.1181	0.1581	0.1981		
		B_Y		0.0441	0.0841	0.1241		
Viewing angle	Hor.	ΘL	CR>10	60	80	--		(1)(4)
		ΘR		60	80	--		
	Ver.	ΘU		60	80	--		
		ΘD		60	80	--		
Option View Direction		Wide angle						

*The data comes from the LCD specification.

Measuring Condition

Measuring surrounding : dark rooms

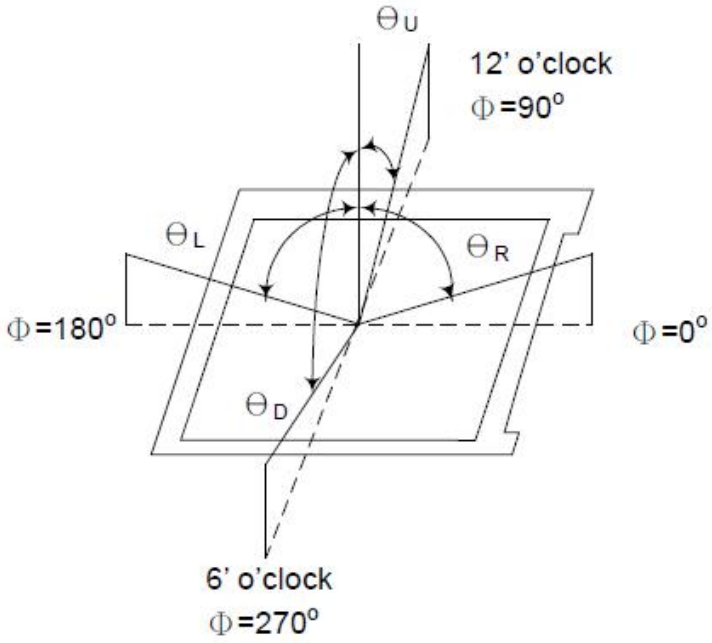
Ambient temperature : 25±2oC

15min. warm-up time.

Measuring Equipment

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

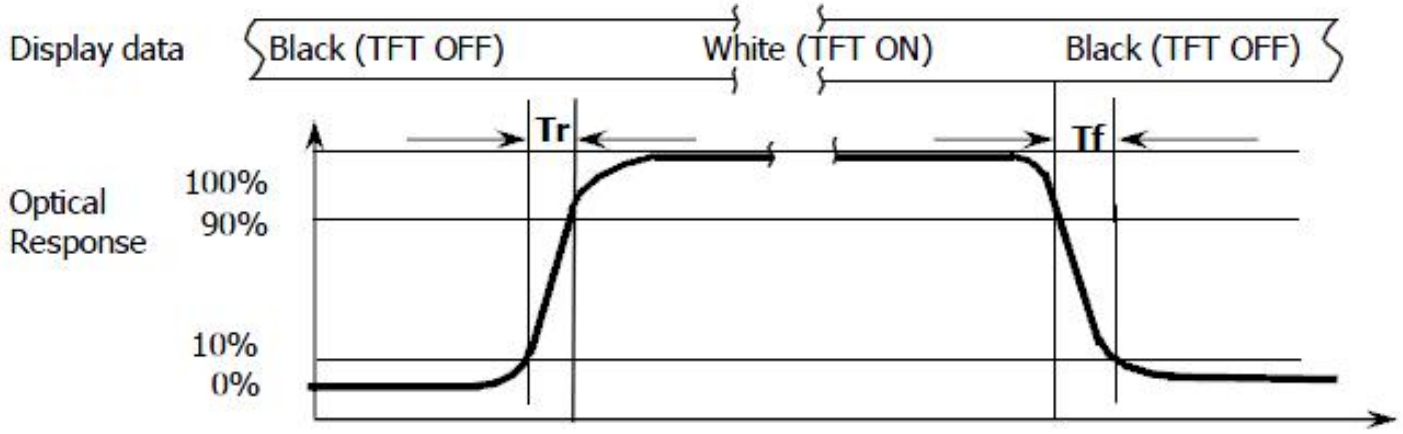
Note (1): Definition of Viewing Angle :



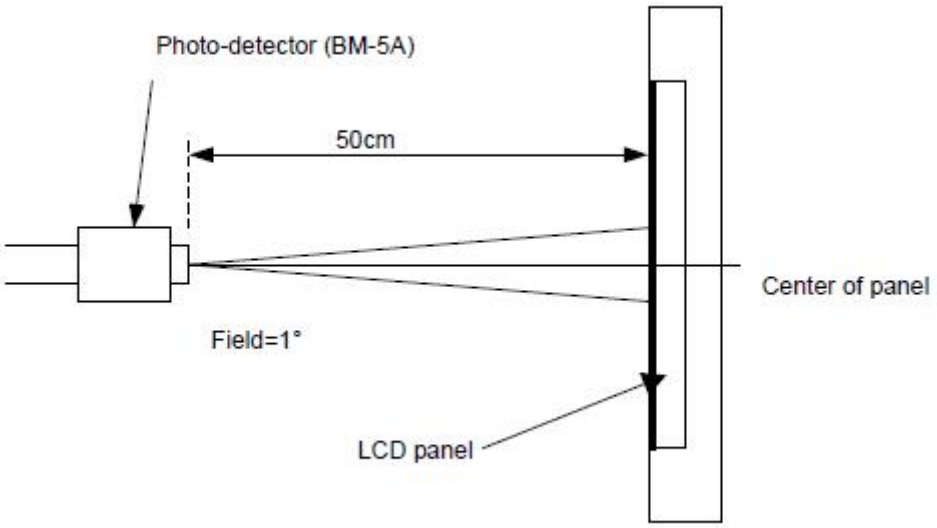
Note (2): Definition of Contrast Ratio(CR) :measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3): Response Time



Note (4): Definition of optical measurement setup



5. Electrical Characteristics

5.1 Absolute Maximum Rating

Characteristics	Symbol	Min.	Max.	Unit	Note
Digital Supply Voltage	VCI	-0.3	4.2	V	Note1
Digital interface supple Voltage	IOVCC	-0.3	3.3	V	Note1
Operating temperature	T_{OP}	-20	+70	℃	
Storage temperature	T_{ST}	-30	+80	℃	

NOTE1: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VCI	2.5	2.8/3.3	3.6	V	
Digital interface supple Voltage	IOVCC	1.65	1.8	3.3	V	
Normal mode Current	IDD	--	5	--	mA	
Level input voltage	V_{IH}	0.7*IOVCC	--	IOVCC	V	
	V_{IL}	GND	--	0.3*IOVCC	V	
Level output voltage	V_{OH}	0.8*IOVCC	--	IOVCC	V	
	V_{OL}	GND	--	0.2*IOVCC	V	

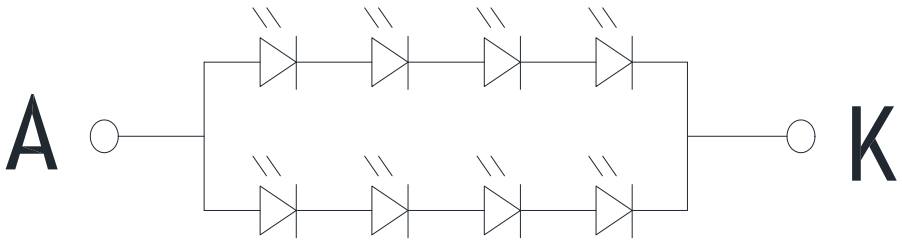
5.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 8 chips LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	30	40	--	mA	
Forward Voltage	V_F	--	12	--	V	
LCM Luminance	LV	300	350	--	cd/m2	Note3
LED life time	Hr	50000	--	--	Hour	Note1,2
Uniformity	Avg	80	--	--	%	Note3

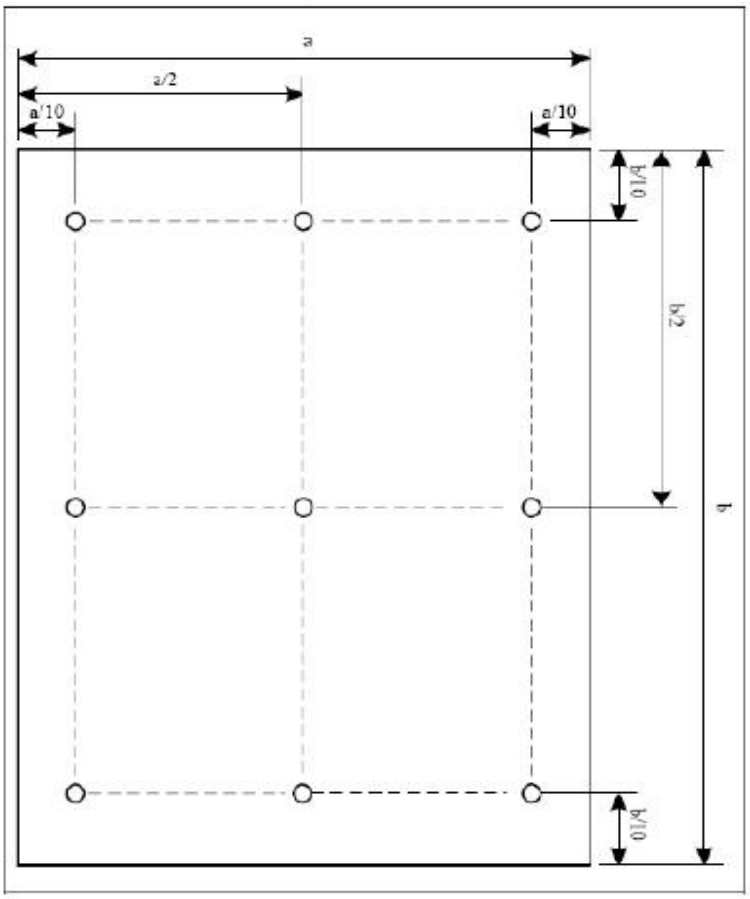
Note1: LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=40mA. The LED lifetime could be decreased if operating IL is larger than 40mA. The constant current driving method is suggested.



B/L Circuit

Note (3) Luminance Uniformity of these 9 points is defined as below:sss

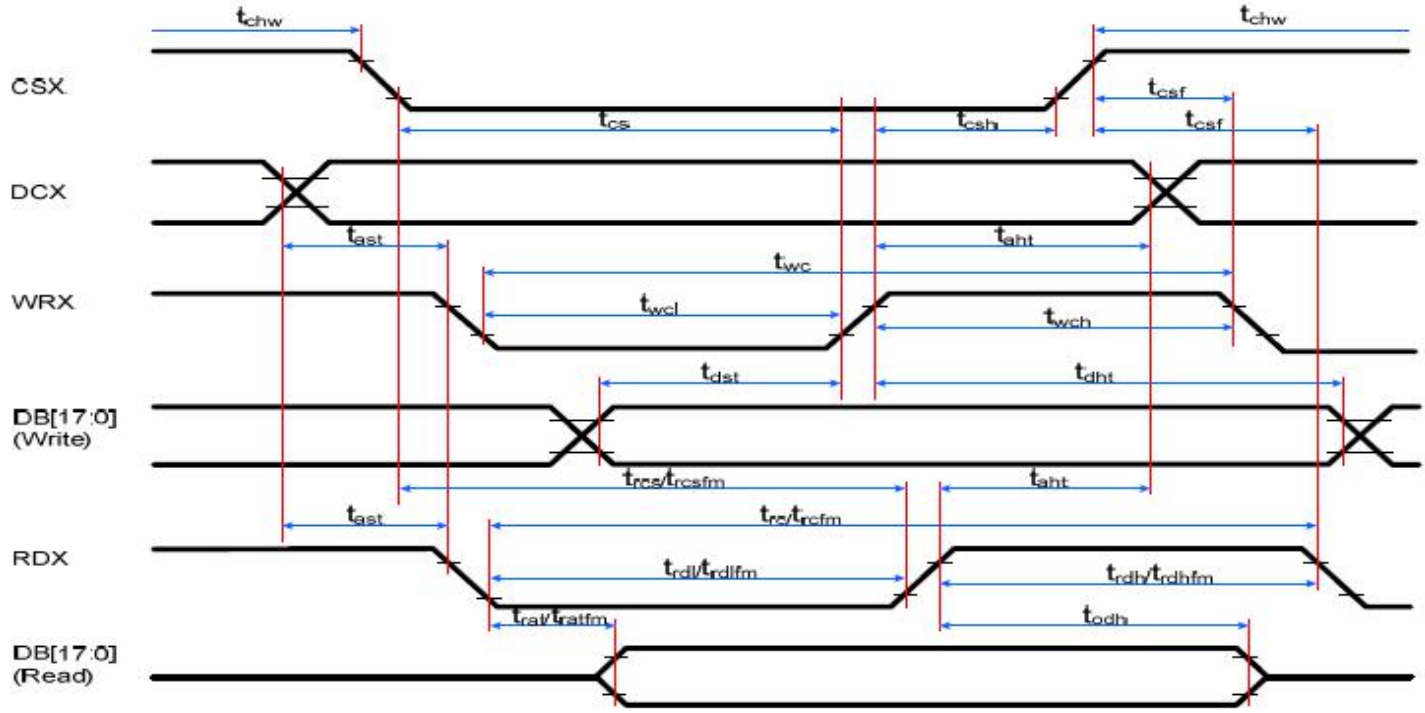


$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

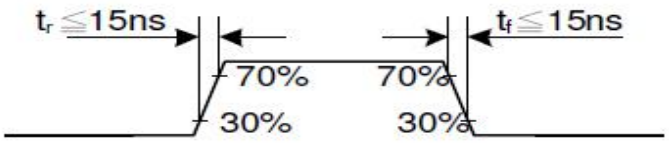
6. AC Characteristics

6.1 Display Parallel 8/9/16/18-bit Interface Timing Characteristics (8080 system)

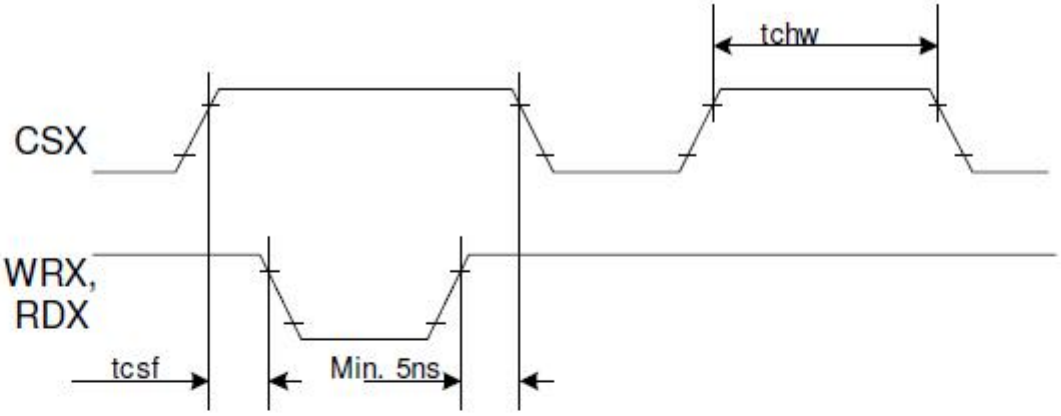


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	10	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[17:10]&D[8:1], D[17:10], D[17:9]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 ℃, IOVCC=1.65V to 2.8V, VCI=2.6V to 3.3V, GND=0V.

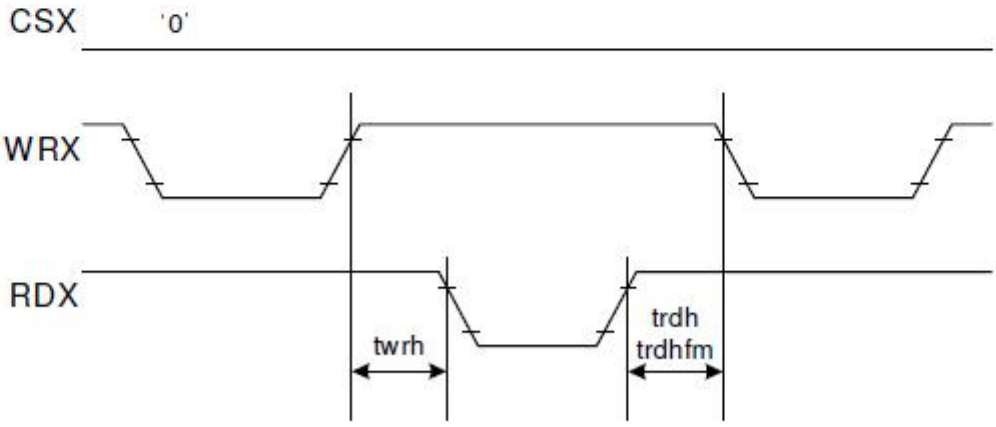


CSX timins :



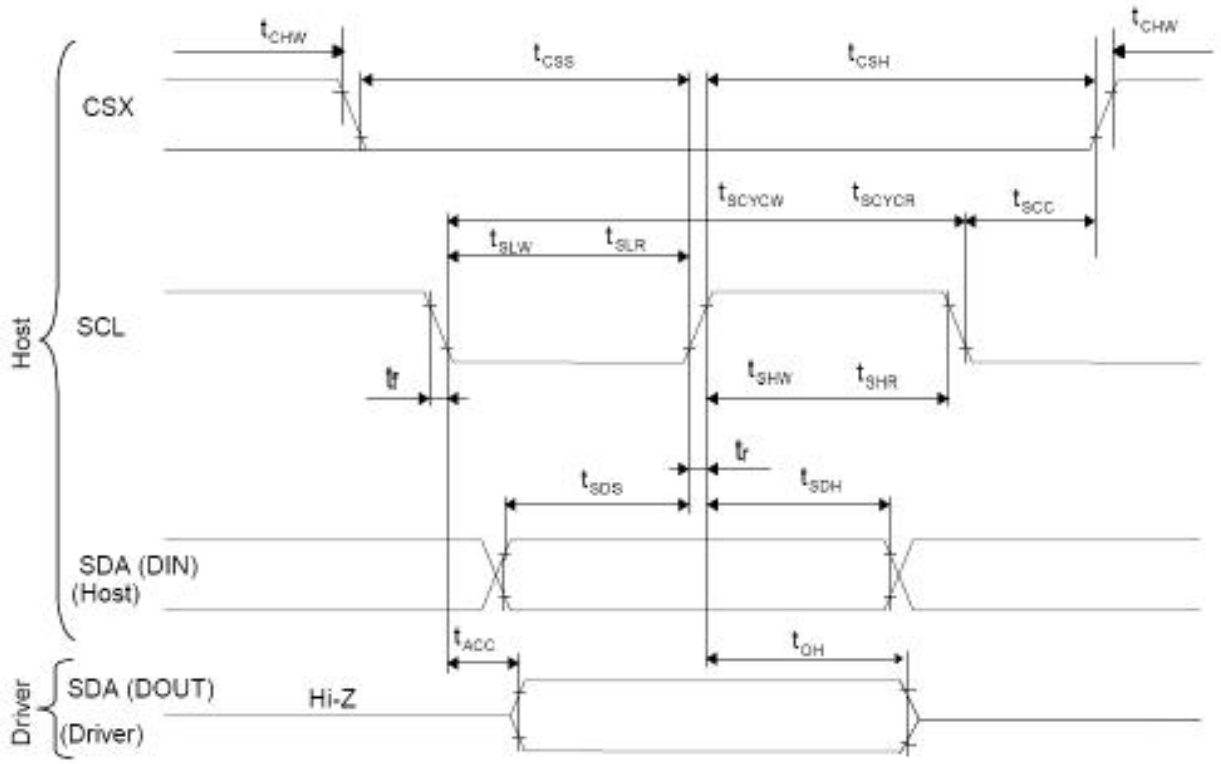
Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Write to read or read to write timings:



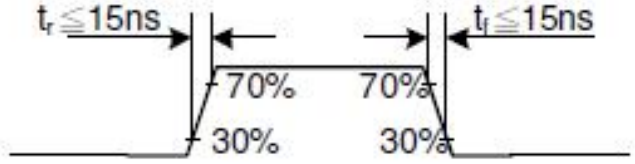
Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

6.2 Display Serial Interface Timing Characteristics (3-line SPI system)

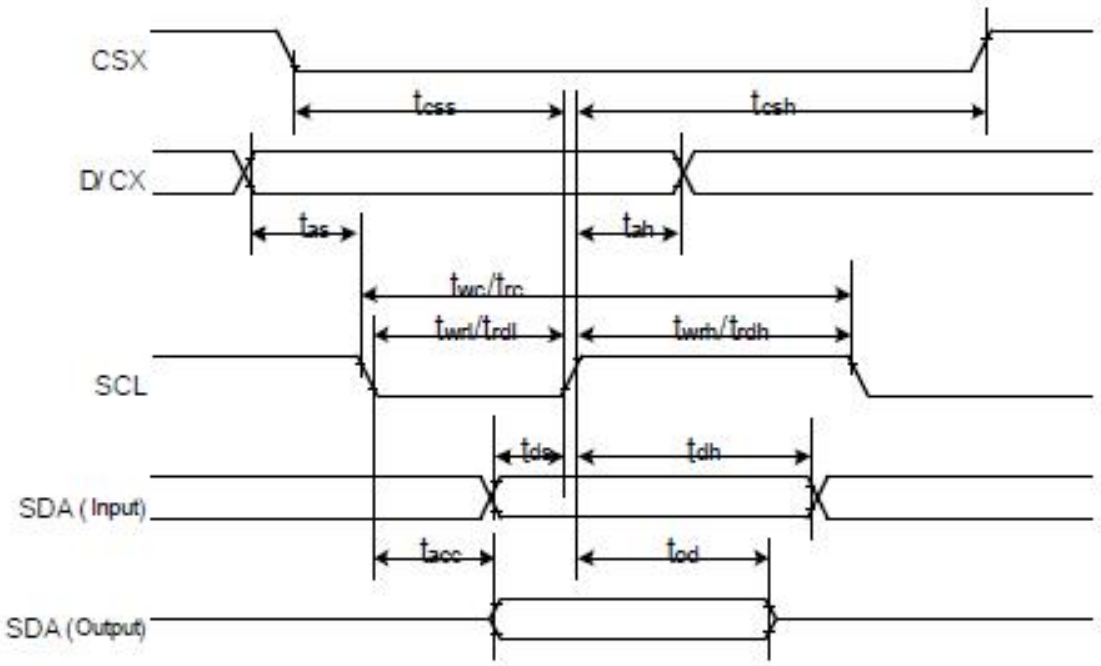


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	35	-	ns	
	tslw	SCL "L" Pulse Width (Write)	35	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	15	50	ns	
CSX	tscc	SCL-CSX	20	-	ns	
	tchw	CSX "H" Pulse Width	40	-	ns	
	tcss	CSX-SCL Time(write)	30	-	ns	
	tcsh		30	-	ns	

Note: Ta = 25 ℃, IOVCC=1.65V to 2.8V, VCI=2.6V to 3.3V, AGND=GND=0V

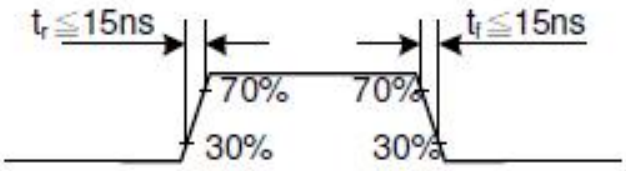


6.3 Display Serial Interface Timing Characteristics (4-line SPI system)

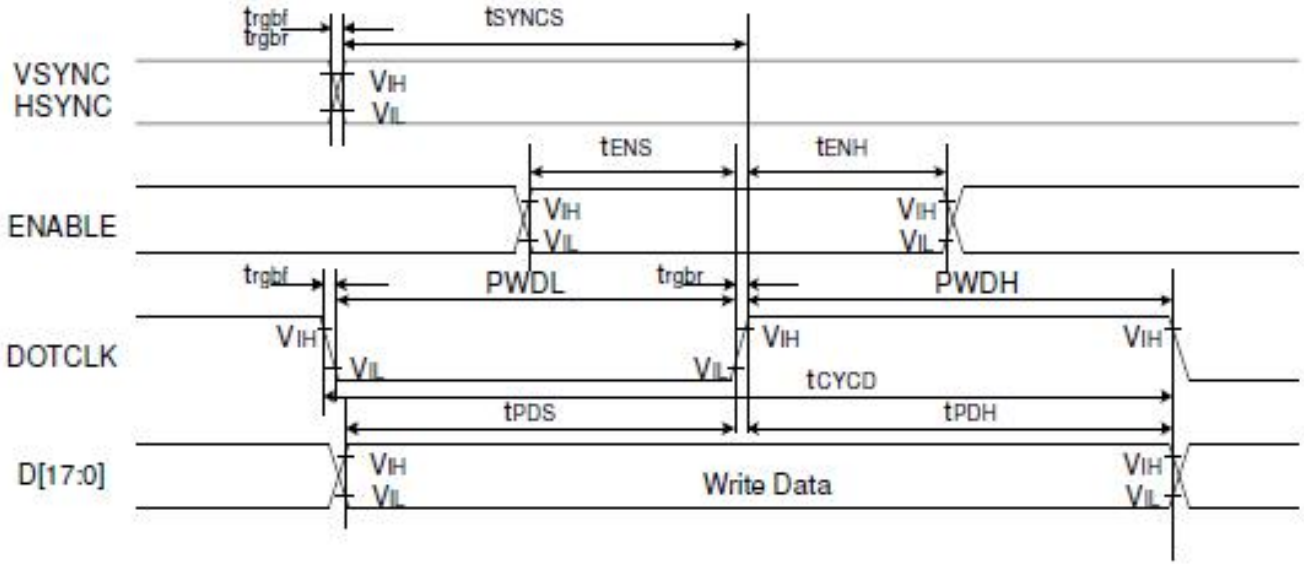


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	30	-	ns	
	tcsh	Chip select hold time (write)	30	-	ns	
SCL	twc	Serial clock cycle (Write)	100	-	ns	
	twrh	SCL "H" pulse width (Write)	35	-	ns	
	twrl	SCL "L" pulse width (Write)	35	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL "H" pulse width (Read)	60	-	ns	
	trdl	SCL "L" pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-		
	tah	D/CX hold time (Write / Read)	10	-		
SDA (Input)	tds	Data setup time (Write)	30	-	ns	
	tdh	Data hold time (Write)	30	-	ns	
SDA (Output)	tacc	Access time (Read)	-	50	ns	For maximum CL=30pF
	tod	Output disable time (Read)	15	50	ns	For minimum CL=8pF

Note: Ta = 25 ℃, IOVCC=1.65V to 2.8V, VCI=2.6V to 3.3V, AGND=GND=0V

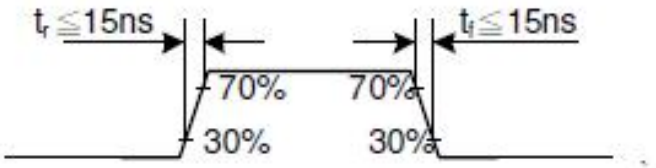


6.4 Parallel 16/18BIT RGB Interface Timing Characteristics



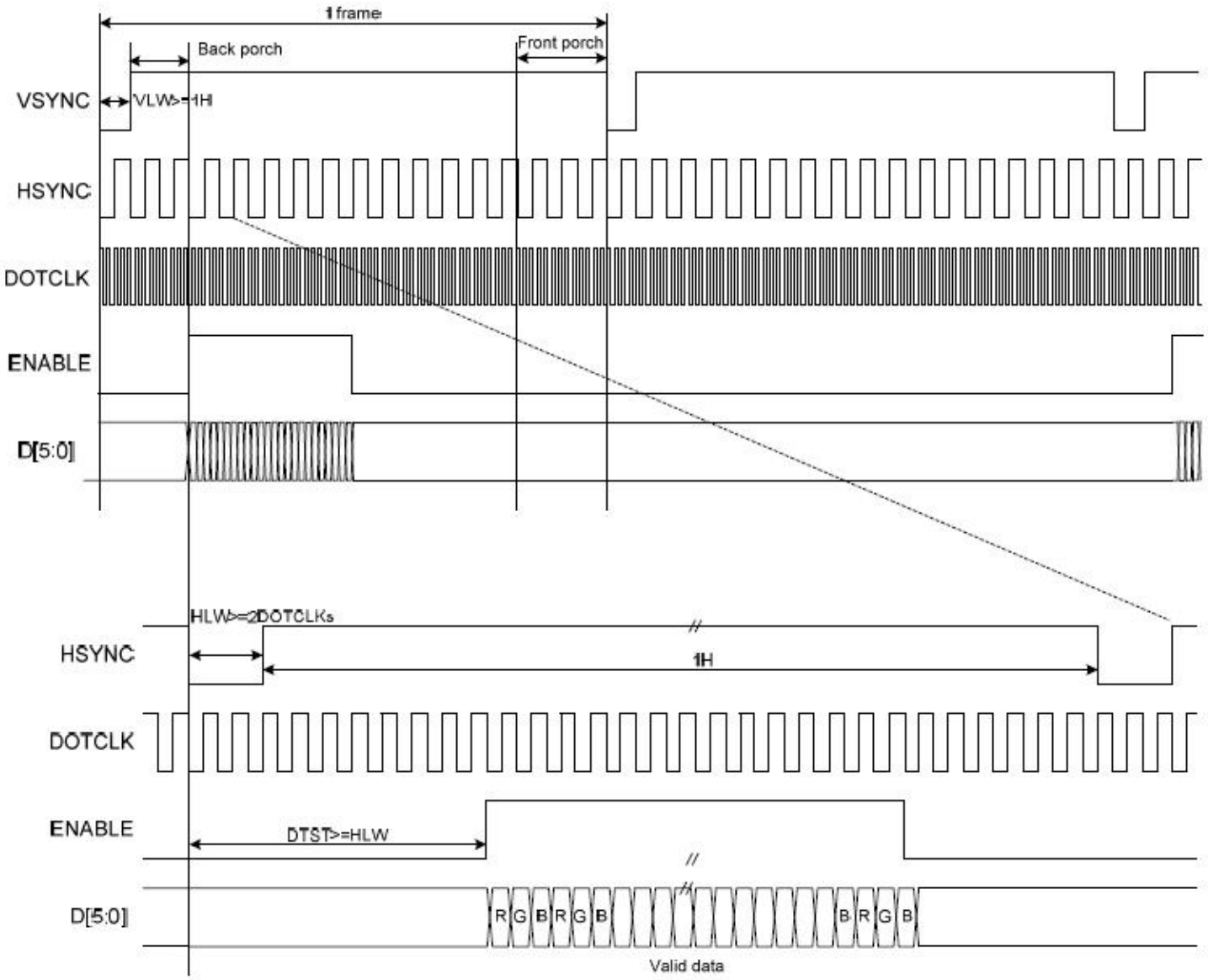
Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{PDS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	33	-	ns	
	PWDL	DOTCLK low-level period	33	-	ns	
	t_{CYCD}	DOTCLK cycle time(18 bit)	100	-	ns	
	t_{rgbr}, t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{PDS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	25	-	ns	
	PWDL	DOTCLK low-level pulse period	25	-	ns	
	t_{CYCD}	DOTCLK cycle time	50	-	ns	
	t_{rgbr}, t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 ℃, IOVCC=1.65V to 2.8V, VCI=2.6V to 3.3V, AGND=GND=0V

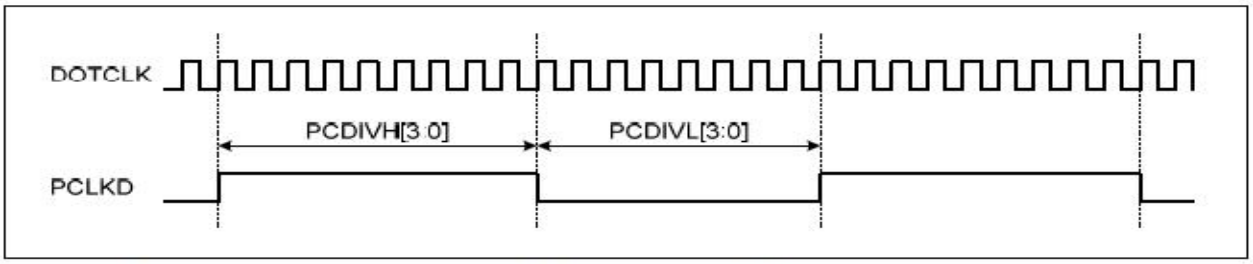


6.5 RGB Interface Timing

The timing chart of 18-/16-bit RGB interface mode is shown as below.



VLW : VSYNC Low Width
HLW : HSYNC Low Width
DTST : Data Transfer Startup Time

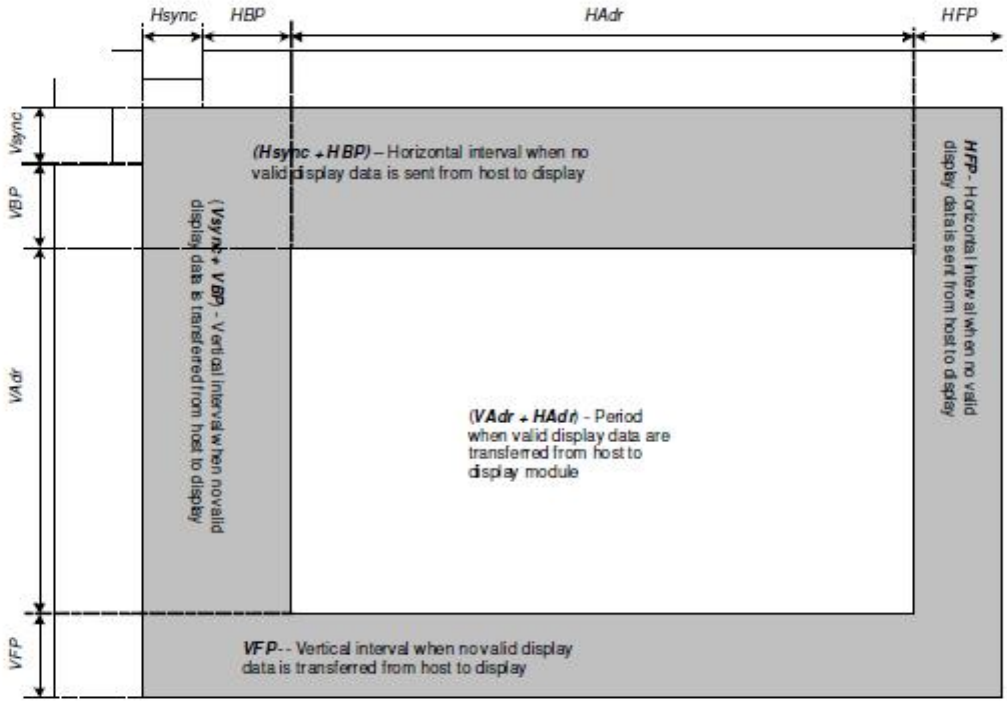


Note 1: The DE signal is not needed when RGB interface SYNC mode is selected.

Note 2: VSPL='0', HSPL='0', DPL='0' and EPL='1' of "Interface Mode Control (B0h)" command.

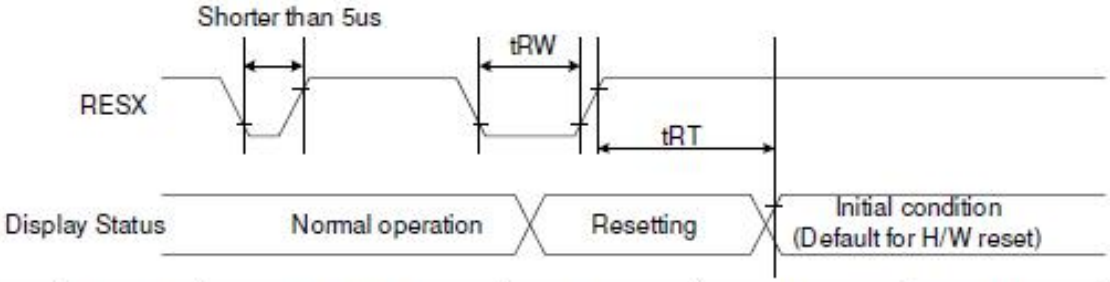
Note 3: In 6-bit RGB interface mode, each dot of one pixel (R, G and B) is transferred in synchronization with DOTCLK.

Note 4: In 6-bit RGB interface mode, set the cycles of VSYNC, HSYNC and DE to 3 multiples of DOTCLK.



Parameters	Symbols	Condition	Min.	Typ.	Max.	Units
Horizontal Synchronization	Hsync		2	10	16	DOTCLK
Horizontal Back Porch	HBP		2	20	24	DOTCLK
Horizontal Back Porch(By pass mode)*	HBP(BP)		58	68	200	DOTCLK
Horizontal Address	HAdr		-	320	-	DOTCLK
Horizontal Front Porch	HFP		2	10	16	DOTCLK
Vertical Synchronization	Vsync		1	2	4	Line
Vertical Back Porch	VBP		1	2	-	Line
Vertical Address	VAdr		-	240	-	Line
Vertical Front Porch	VFP		3	4	-	Line

6.6 Reset Timing Characteristics



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

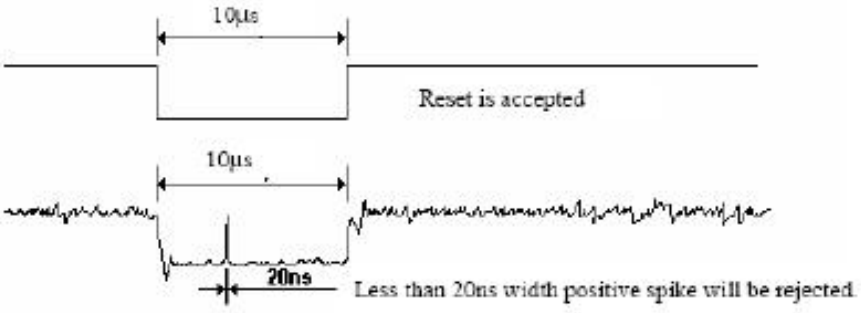
Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NV memory to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below: -

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In -mode.) And then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5: When Reset applied during Sleep In Mode.

Note 6: When Reset applied during Sleep Out Mode.

Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7. LCD Module Out-Going Quality Level

7.1 VISUAL & FUNCTION INSPECTION STANDARD

7.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

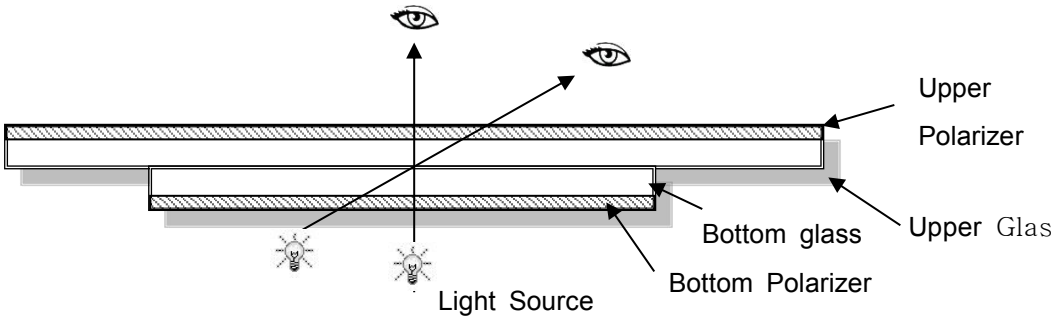
Temperature : 25±5℃

Humidity : 65%±10%RH

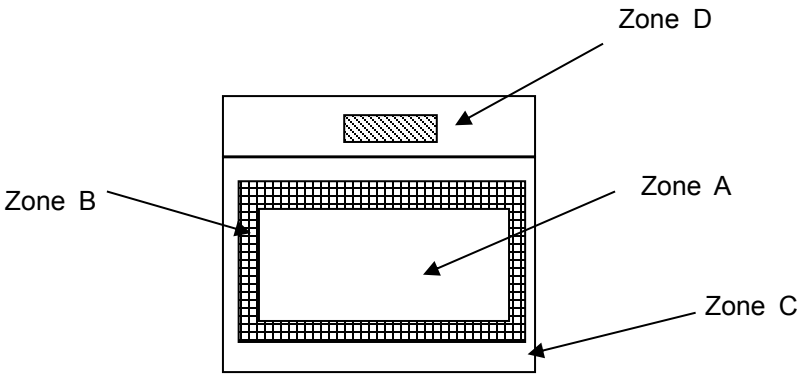
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm



7.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Zone D : IC Bonding Area

Note:As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer

7.1.3 Sampling Plan

According to GB/T 2828.1-2003 ; , normal inspection, Class Ⅱ

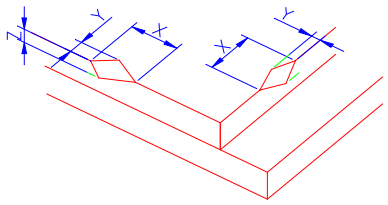
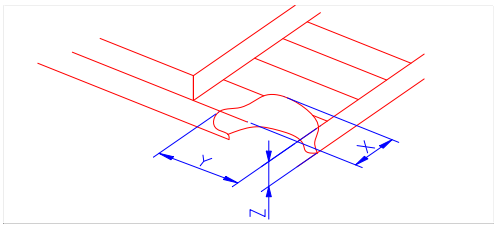
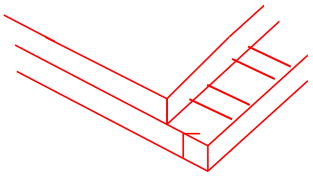
AQL:

Major defect	Minor defect
0.65	1.5

LCD: Liquid Crystal Display , TP: Touch Panel , LCM: Liquid Crystal Module

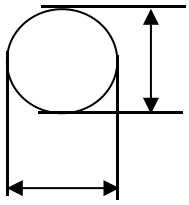
No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot Line defect	Light dot，Dim spot,Polarizer Bubble ; Polarizer accidented spot.	
6	Soldering appearance	Good soldering , Peeling off is not allowed.	
7	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	

7.1.4 Criteria (Visual)

<table>
<tr><th>Number</th><th>Items</th><th>Criteria(mm)</th></tr>
<tr><td rowspan="3">1.0 LCD Crack/Broken
NOTE:
X: Length
Y: Width
Z: Height
L: Length of ITO,
T: Height of LCD</td><td>(1) The edge of LCD broken</td><td> 
<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr></table></td></tr>
<tr><td>(2)LCD corner broken</td><td> 
<table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table></td></tr>
<tr><td>(3) LCD crack</td><td> 
Crack
Not allowed</td></tr>
</table>

2.0

Spot defect



Φ=(X+Y)/2

① light dot（LCD/TP/Polarizer black/white spot , light dot, pinhole, dent, stain）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.10	Ignore		Ignore
0.10<Φ≤0.20	3(distance≧10mm)		
0.20<Φ≤0.25	2		
Φ>0.3	0		

②Dim spot（LCD/TP/Polarizer dim dot, light leakage、dark spot）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.1	Ignore		Ignore
0.10<Φ≤0.20	3(distance≧10mm)		
0.20<Φ≤0.25	2		
Φ>0.3	0		

③ Polarizer accidented spot

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.3<Φ≤0.5	2(distance≧10mm)		
Φ>0.5	0		

④Pixel bad points（light dot，Dim dot, color dot）

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.1	Ignore		Ignore
0.15<Φ≤0.2	2(distance≧10mm)		
Φ>0.2	0		

⑤ Polarizer Bubble

Zone / Size (mm)	Acceptable Qty		
	A	B	C
Φ≤0.2	Ignore		Ignore
0.3<Φ≤0.4	3(distance≧10		
0.4<Φ≤0.5	2		
Φ>0.5	0		

<table>
<tr><td>3.0</td><td>Line defect (LCD/ TP /Polarizer backlight black/white line, scratch, stain)</td><td>
<table>
<tr><td rowspan="2">Width(mm)</td><td rowspan="2">Length(mm)</td><td colspan="3">Acceptable Qty</td></tr>
<tr><td>A</td><td>B</td><td>C</td></tr>
<tr><td>Φ≤0.03</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.03<W≤0.04</td><td>L≤3.0</td><td colspan="2">N≤2</td></tr>
<tr><td>0.04<W≤0.05</td><td>L≤2.0</td><td colspan="2">N≤1</td></tr>
<tr><td>0.05<W</td><td colspan="4">Define as spot defect</td></tr>
</table>
</td></tr>
<tr><td>4.0</td><td>Electronic Components SMT</td><td>Not allow missing parts，solderless connection，cold solder joint，mismatch，The positive and negative polarity opposite</td></tr>
<tr><td>5.0</td><td>Display color& Brightness</td><td>1. Color：Measuring the color coordinates, The measurement standard according to the datasheet or samples.
2. Brightness：Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.</td></tr>
<tr><td>6.0</td><td>LCD Mura</td><td>By 5% ND filter invisible.</td></tr>
</table>

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed

8. Reliability Test Result

Item	Condition	Inspection after test
High Temperature Operating	70℃,96H	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD; 2.Non-display; 3.Missing segments/line; 4.Glass crack; 5.Current IDD is twice higher than initial value.
Low Temperature Operating	-20℃, 96HR	
High Temperature Storage	80℃, 96HR	
Low Temperature Storage	-30℃, 96HR	
High Temperature & High Humidity Operating	+60℃, 90% RH ,96 hours.	
Thermal Shock (Non-operation)	-10℃,30 min ↔ +60℃,30 min, Change time:5min 20CYC.	
ESD test	C=150pF, R=330,5points/panel Air:±8KV, 5times; Contact:±6KV, 5 times; (Environment: 15℃~35℃, 30%~60%).	
Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	
Box Drop Test	1 Corner 3 Edges 6 faces,80㎝(MEDIUM BOX)	

Remark:

1.The test samples should be applied to only one test item.

2.Sample size for each test item is 5~10pcs.

3.For Damp Proof Test, Pure water(Resistance＞10MΩ) should be used.

4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.

5.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

6. The color fading mura of polarizing filter should not care.

9. Cautions and Handling Precautions

9.1 Handling and Operating the Module

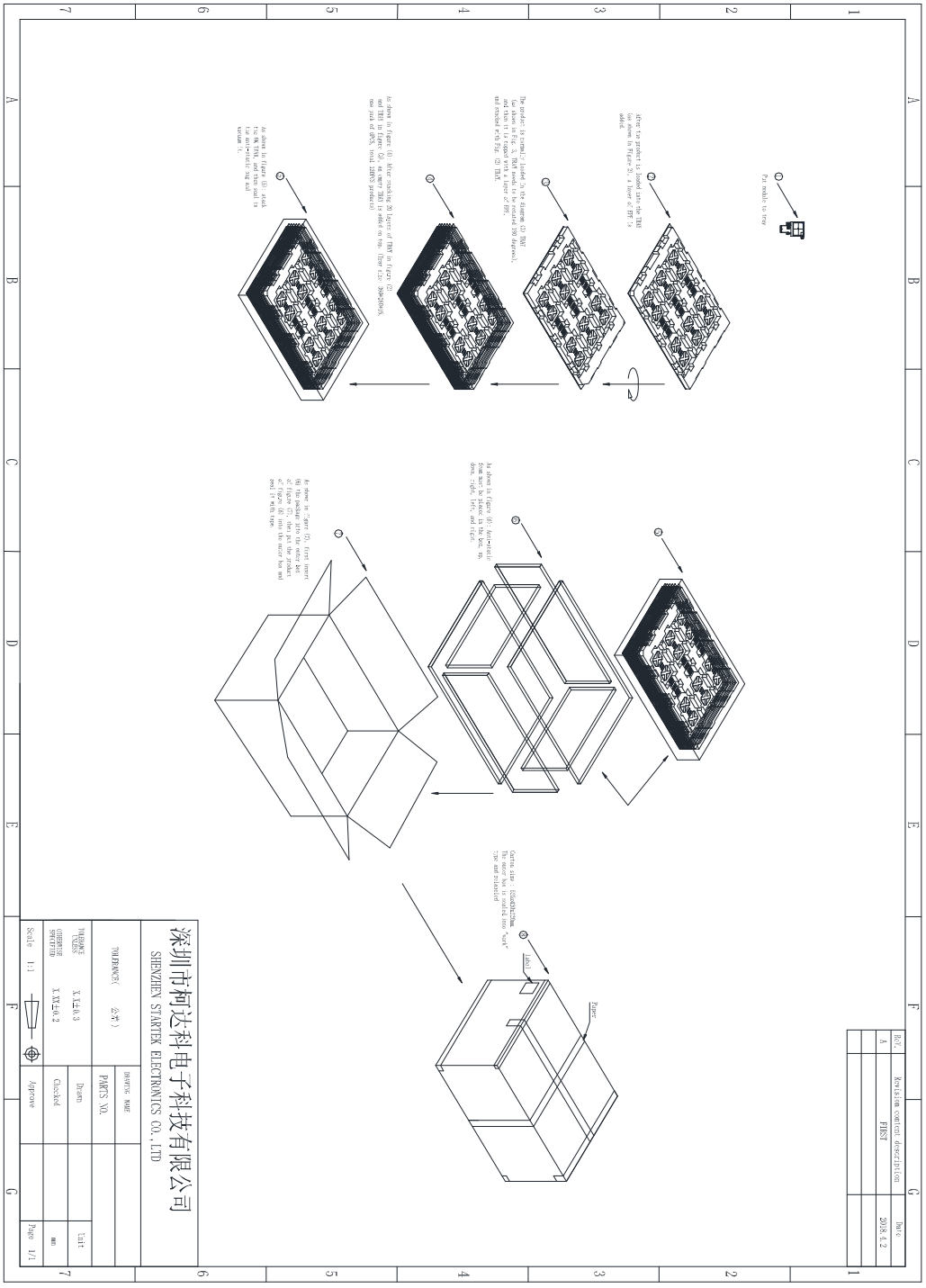
(1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
(4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
(8) Protect the module from static; it may cause damage to the CMOS ICs.
(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
(10) Do not disassemble the module.
(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
(12) Pins of I/F connector shall not be touched directly with bare hands.
(13) Do not connect, disconnect the module in the “Power ON” condition.

9.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
(2) Do not store the TFT-LCD module in direct sunlight.
(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.

(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

10. Packing


深圳市柯达科电子科技有限公司
SHENZHEN STARTEK ELECTRONICS CO.,LTD
Label
Paper